Patent
Attorney's Docket No. 032908-008

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

UTILITY PATENT
APPLICATION TRANSMITTAL LETTER

Box PATENT APPLICATION
Assistant Commissioner for Patents
Washington, D.C. 20231

Sir:

Enclosed for filing is the utility patent application of Nadim F. Haddad, Frederick T. Brady and Jonathan Maimon for Method to Harden Shallow Trench Isolation Against Total Ionizing Dose Radiation.

Also enclosed are:

[X] 3 sheet(s) of [ ] formal [ ] informal drawing(s);

[ ] a claim for foreign priority under 35 U.S.C. §§ 119 and/or 365 is [ ] hereby made to _ filed in _ on _;
[ ] in the declaration;

[ ] a certified copy of the priority document;

[ ] a General Authorization for Petitions for Extensions of Time and Payment of Fees;

[ ] _____ statement(s) claiming small entity status;

[ ] an Assignment document;

[ ] an Information Disclosure Statement; and

[ ] Other: _____.

[X] An [ ] executed [X] unexecuted declaration of the inventor(s)
[ ] also is enclosed [ ] will follow.

[ ] Please amend the specification by inserting before the first line the sentence --This application claims priority under 35 U.S.C. §§119 and/or 365 to _ filed in _ on _; the entire content of which is hereby incorporated by reference.--

[ ] A bibliographic data entry sheet is enclosed.

[X] The filing fee has been calculated as follows [ ] and in accordance with the enclosed preliminary amendment:

CLAIMS					
	NO. OF CLAIMS		**EXTRA CLAIMS**	**RATE**	**FEE**
Basic Application Fee					$690.00 (101)
Total Claims	12	MINUS 20 =	-0-	x $18.00 (103)	-0-
Independent Claims	2	MINUS 3 =	-0-	x $78.00 (102)	-0-
If multiple dependent claims are presented, add $260.00 (104)					-0-
Total Application Fee					690.00
If verified Statement claiming small entity status is enclosed, subtract 50% of Total Application Fee					-0-
Add Assignment Recording Fee if Assignment document is enclosed					-0-
TOTAL APPLICATION FEE DUE					**690.00**

[ ] This application is being filed without a filing fee. Issuance of a Notice to File Missing Parts of Application is respectfully requested.

[ ] A check in the amount of $ _____ is enclosed for the fee due.

[X] Charge $ 690.00 to Deposit Account No. 02-4800 for the fee due.

[X] The Commissioner is hereby authorized to charge any appropriate fees under 37 C.F.R. §§ 1.16, 1.17 and 1.21 that may be required by this paper, and to credit any overpayment, to Deposit Account No. 02-4800. This paper is submitted in duplicate.

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Respectfully submitted,

BURNS, DOANE, SWECKER & MATHIS, L.L.P.

Date: July 31, 2000

By: _____
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CONFIDENTIAL

APPLICATION FOR UNITED STATES LETTERS PATENT

by

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FREDERICK T. BRADY

and

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for

METHOD TO HARDEN SHALLOW TRENCH ISOLATION AGAINST TOTAL IONIZING DOSE RADIATION

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Attorney Docket No. 032908-008

CONFIDENTIAL

METHOD TO HARDEN SHALLOW TRENCH ISOLATION AGAINST TOTAL IONIZING DOSE RADIATION

This disclosure is based upon, and claims priority from, provisional U.S. Patent Application No. 60/146,895, filed August 2, 1999, the contents of which are incorporated herein by reference.

BACKGROUND OF THE INVENTION

1. Technical Field

The present invention relates to integrated circuits in general, and in particular to a method for fabricating integrated circuit devices. Still more particularly, the present invention relates to an enhanced shallow trench isolation method for fabricating radiation-tolerant integrated circuit devices.

2. Description of the Prior Art

Within a semiconductor integrated circuit (IC) device, device isolation regions can typically be found between two adjacent active components to prevent carriers from traveling between the two adjacent active components. For example, device isolation regions are conventionally formed between two adjacent field effect transistors (FETs) to reduce charge leakage to and from the two FETs. Often, device isolation regions take the form of thick field oxide regions extending below the surface of a semiconductor substrate. The most common technique for forming a thick field oxide region is to use a local oxidation of silicon (LOCOS) processing technique that is well-known to those skilled in the art of semiconductor processing. Details related to the LOCOS processing techniques can be found in *VLSI technology*, S. M. Sze, McGraw-Hill, 1983, which is incorporated by reference herein.

However, bird's beak regions formed in the LOCOS growth of field oxide regions are undesirable because they are typically too thin to provide any impact in terms of device isolation. Bird's beak regions nevertheless consume substrate surface area, limiting the extent to which the field oxide region can be shrunk while still providing desirable levels of device isolation. To provide higher device densities, it is therefore desirable to utilize a better device isolation structure such as shallow trench isolation (STI). With STI technology, a sharply defined trench is formed in the semiconductor substrate by, for example, anisotropic etching. The trench is filled with oxide back to the surface of a semiconductor substrate to provide a device isolation region. Trench isolation regions formed by STI have the advantages of providing device isolation across their entire lateral extent and of providing a more planar structure.

The present disclosure provides an improved STI method for fabricating a shallow trench that yields a desirable level of radiation tolerance so that the resulting semiconductor IC device can be used in high-radiation environments. Radiation tolerance refers to the ability of a semiconductor IC device to withstand radiation without alteration of its electrical characteristics. A semiconductor IC device is said to be radiation tolerant if it can continue to function within specifications after exposure to a specified amount of radiation.

SUMMARY OF THE INVENTION

In accordance with a preferred embodiment of the present invention, a layer of pad oxide is first deposited on a semiconductor substrate. A layer of pad nitride is then deposited on the pad oxide layer. A trench is defined within the semiconductor substrate by selectively etching the pad nitride layer, the pad oxide layer, and the semiconductor substrate. Boron ions are then implanted into both the bottom and along the sidewalls of the trench. Subsequently, a trench plug is formed within the trench by depositing an insulating material into the trench and by removing an excess portion of the insulating material. Since the boron ions are implanted at an angle during the above-mentioned ion implantation step, the semiconductor IC device advantageously exhibits enhanced radiation-tolerance.

As further steps, a p-well is implanted to a depth just below the depth of the bottom of the trench. This helps to keep the threshold voltage of the IC device below the trench at a high level, and thereby keep post-radiation leakage low. Then, an electrically neutral species is implanted into the wafer. This implant can be a blanket implant over the whole wafer, or p-channel devices can be shielded from the implant.

Each of these steps can be individually employed to increase radiation hardness over conventional levels. However, the best results are achieved when all of the steps are employed in conjunction with one another.

BRIEF DESCRIPTION OF THE DRAWINGS

The invention itself, as well as a preferred mode of use, further objects, and advantages thereof, will best be understood by reference to the following detailed description of an illustrative embodiment when read in conjunction with the accompanying drawings, wherein:

Figure **1** is a pictorial diagram of a semiconductor substrate having a layer of pad oxide and a layer of pad nitride, in accordance with a preferred embodiment of the present invention;

Figure **2** illustrates the formation of a trench definition mask on the semiconductor substrate from Figure **1**, in accordance with a preferred embodiment of the present invention;

Figure **3** illustrates the formation of a trench on the semiconductor substrate from Figure **1**, in accordance with a preferred embodiment of the present invention;

Figure **4** is a pictorial illustration of the directional boron implantations, in accordance with a first aspect of the present invention;

Figures **5-8** illustrate the formation of a trench plug on the semiconductor substrate from Figure **1**, in accordance with a preferred embodiment of the present invention;

Figure **9** illustrates the formation of a P-well, in accordance with a second aspect of the invention; and

Figure **10** illustrates the implantation of an electrically neutral material, in accordance with a third aspect of the invention.

DETAILED DESCRIPTION OF A PREFERRED EMBODIMENT

The present invention provides an enhanced shallow trench isolation (STI) method for fabricating radiation tolerant semiconductor integrated circuit (IC) devices, and a preferred embodiment will be described in detail with reference to the accompanying drawings. The fabrication process begins with the division of a semiconductor substrate into active regions where active electrical components are to be formed, and isolation regions that electrically separate the active regions.

Referring now to the drawings and in particular to Figure **1**, there is illustrated a pictorial diagram of a semiconductor substrate having a layer of pad oxide and a layer of pad nitride, in accordance with a preferred embodiment of the present invention. As shown, a silicon substrate **10** is coated with a layer of thermal oxide that acts as a pad oxide layer **11**. Pad oxide layer **11** protects the surface of substrate **10** from damage in subsequent processing steps. For this purpose, the pad oxide layer has a thickness of approximately 100Å - 300Å. In addition, a layer of silicon nitride that serves as a pad nitride layer **12** is formed on top of pad oxide layer **11**. Pad nitride layer **12** may be deposited by chemical vapor deposition (CVD) to a thickness of 1000-3000 Å.

Next, a trench definition mask **14**, as depicted in Figure **2**, is formed by exposing and etching a layer of photoresist that was deposited onto pad nitride layer **12**. Trench definition mask **14** is shaped in the usual manner

so that the surface of pad nitride layer **12** is exposed at a region **x** where a trench will be formed. Trench definition mask **14** may itself be used as the mask for etching layers **12** and **11** as well as substrate **10** in forming a trench, or trench definition mask **14** may be used to define a mask in pad nitride layer **12** that can then be used for subsequent etching steps. Most often, a photoresist mask is used to define the lateral extent of all of the etching steps used in the formation of a trench in substrate **10** because fewer processing steps are involved.

A trench **15** is then formed in substrate **10**, as illustrated in Figure **3**, by consecutively etching pad nitride layer **12**, pad oxide layer **11**, and substrate **10**. The etching processes used are preferably anisotropic and may, for example, be performed by reactive ion etching (RIE). For example, a gas etchant, such as CF_4 and O_2, is used to etch pad nitride layer **12** and pad oxide layer **11**. Substrate **10** is etched using RIE and a mixture of gases including Cl_2, O_2, HBr, and He. The bottom portion of trench **15** can be etched using SF_6 so that the transition between the bottom and sidewalls of trench **15** is rounded. An appropriate trench depth for forming a shallow trench isolation is approximately 2000Å-5000Å deep. Trench definition mask **14** can be removed at this point. If desired, a thin thermal oxide layer (*i.e.*, sidewall oxide) may be grown on the sidewalls and bottom of trench **15** to remove any defects created by the etching processes. If such a thin thermal oxide layer is formed, the thin thermal oxide layer may either be left in place to become part of a trench plug (such as trench plug **17** shown in Figure **6**) or be removed.

With reference now to Figure **4**, there is illustrated a pictorial illustration of directional boron ion implantations, in accordance with one

aspect of the present invention. As indicated by arrows **31**, boron ions are first introduced at an angle in a range of about 0°-7° from a vertical axis. Subsequently, a second implantation **32** at a higher angle, in the range of 30°-45°, is carried out. The boron ion implantation steps preferably have the following parameters: an energy in a relatively low range of about 20 KeV or less, and a concentration of boron ions in a range between approximately 10^{10} atoms/cm^2 and 10^{13} atoms/cm^2. If there is a sidewall oxide deposited within trench **15**, the energy of the boron ion implantation should be high enough for the boron ions to penetrate through the sidewall oxide and stop in substrate **10**. Also shown in Figure **4** is the area of boron ion implantation within substrate **10**, which is marked by a dotted line **33**.

The low-angle implant provides a high pre-radiation threshold voltage beneath the trench. Hence, even if a substantial amount of positive charge is trapped in the trench during irradiation, the field threshold remains high, and no radiation-induced leakage occurs between neighboring n-channel transistors. The higher-angle implant provides similar results to create a high threshold voltage along the side walls of the trench. This helps to keep radiation-induced leakage low along the parasitic sidewall path that typically occurs between the source and drain within an n-channel transistor.

The implantation of the boron ions at an angle into the field isolation area can be carried out in a number of different ways. For example, an ion beam generator can be mounted in a manner such that it can be pivoted relative to the semiconductor substrate, to emit a beam of ions at any desired angle relative to the substrate. More preferably, however, the substrate is mounted on a pivoted or gimbaled platform, so that its orientation relative to a fixed ion beam generator can be varied during the implantation process, to

receive the beam of ions at the desired angle. Further, although two separate implantation steps have been described for the bottom and side walls of the trench, a single continuous implantation could be carried out as well. If desired, conventional lithography techniques can be used to protect p-channel areas from the boron implant.

Next, trench **15** is filled with a layer of silicon oxide **16** by, for example, low pressure chemical vapor deposition (LPCVD) using tetraethylortho-siloxane (TEOS) as a source gas. Trench **15** is overfilled during deposition, as shown in Figure **5**, in order to achieve good planarization during subsequent CMP process and to account for possible densification. Densification of the TEOS oxide is preferably accomplished at a temperature of approximately 1000°C for 10-30 minutes. After densification, the portion of the TEOS oxide layer extending above pad nitride layer **12** is removed by chemical mechanical polishing (CMP) using pad nitride layer **12** as a stop for the polishing process. After the CMP process, some oxide is left inside trench **15** to form a trench plug **17**, as depicted in Figure **6**. Although not clearly shown in Figure **6**, the surface of trench plug **17** is recessed slightly below the surface of pad nitride layer **12** after the CMP process because the silicon oxide in trench plug **17** is softer than the silicon nitride in pad nitride layer **12**.

Pad nitride layer **12** is subsequently removed to expose pad oxide layer **11**, typically leaving a portion of trench plug **17** extending above the surface of pad oxide layer **11**, as illustrated in Figure **7**. A hydrofluoric acid dip is then used to remove pad oxide layer **11**, resulting a structure shown in Figure **8**. A greater depth of trench plug **17** than that of pad oxide layer **11** is removed during this etching process because trench plug **17**, which is

formed of TEOS, is etched more rapidly than pad oxide layer **11**, which is formed of thermal oxide.

A sacrificial oxide layer **18** is grown on the surface of substrate **10** for protecting the surface of substrate **10** and for limiting the channeling of ions implanted in subsequent ion implantation steps. A p-type dopant, such as boron or indium, is then implanted to form a P-well 19, as depicted in Figure **9.** As a second feature of the invention, the energy of the implant is determined so that the depth of the well **19** is just below the bottom of the trench **15.** This arrangement helps to keep the threshold beneath the trench at a high level, so that post-radiation leakage remains low.

In an embodiment of the invention where the P-well is formed by a boron implant, the step of implanting the boron can be carried out in conjunction with, or as part of, the low-angle boron implant **31** that occurs prior to filling the trench. Also, conventional photolithography processes can be used to cover p-channel devices during this implant.

As a third step in the radiation hardening of the IC device, an electrically neutral species, such as germanium, is implanted into the wafer. In carrying out this step, a blanket implant can be performed over the entire wafer, as shown in Figure **10**, or photolithography techniques can be employed to shield p-channel devices from the implanted ions. Preferably, high dosage levels are used for this implant, for example around 10^{13} atoms/cm^2 or higher. The implant energy is adjusted to correspond to the implant depth of the n-channel transistors **34**, or both n- and p-channels if a blanket implant is utilized. More specifically, the energy of the implant should be regulated to limit the implantation to a depth **35** which ensures that the

electrically neutral species remain in the n^+ and p^+ diffusion regions. If the implant extends into the junction between these diffusion regions and the well, the diode which results from this junction could be leaky.

Sacrificial oxide layer **18** is subsequently removed, once again using a hydrofluoric acid dip. The semiconductor substrate is thereafter subjected to further processing to complete a fabrication of a semiconductor IC device. A description of those further processing steps, which are known to those skilled in the relevant art, is not necessary to an understanding of the present invention, and therefore not presented herein.

As has been described, the present invention provides an enhanced STI method for fabricating radiation-tolerant IC devices. The increase in radiation tolerance is attributable to the implantation of boron ions at an angle during an boron ion implantation step. As a result, a higher p-type concentration can be maintained under the field oxide regions of the substrate. Because of the high p-type concentration in the substrate, the substrate is able to withstand a relatively high dose of radiation before any inversion occurs at the surface of the substrate. Further enhancements are provided by implanting the p-well to a depth just below the bottom of the trench, and by implanting an electrically neutral species into the wafer. In view of such, IC devices that are fabricated using the present invention exhibit enhanced radiation-tolerance.

While the invention has been particularly shown and described with reference to a preferred embodiment, it will be understood by those skilled in the art that various changes in form and detail may be made therein without departing from the spirit and scope of the invention.

CLAIMS

What is claimed is:

1. A method for fabricating radiation-tolerant integrated circuit devices, said method comprising:

depositing a layer of pad oxide on a semiconductor substrate;

selectively etching said pad oxide layer and said semiconductor substrate to define a trench within said semiconductor substrate; and

implanting boron ions at an angle with respect to normal in said trench.

2. The method according to Claim 1, wherein said boron ions are implanted beneath the bottom of the trench and along the side walls of the trench.

3. The method according to Claim 1, wherein said boron ion implantation is performed with an energy no greater than about 20 KeV.

4. The method according to Claim 1, wherein said boron ion implantation is performed with a dose of boron ions in a range between approximately 10^{10} atoms/cm^2 and 10^{13} atoms/cm^2.

5. The method according to Claim 1, further including the step of implanting a p-type material to form a P-well having a depth greater than the depth of said trench.

6. The method according to Claim 5, further including the step of implanting an electrically neutral material into said substrate.

7. The method according to Claim 6, wherein said electrically neutral material is implanted to a depth which is no greater than the depth of a diffusion region in said P-well.

8. A semiconductor integrated circuit device, comprising:

a semiconductor substrate having a layer of pad oxide and a patterned pad nitride; and

a shallow trench formed within said semiconductor substrate, which includes a implantation region formed by implanting boron ions below the bottom and along the side walls of said shallow trench.

9. The semiconductor integrated circuit device according to Claim 8, further including a P-well having a depth which is greater than the depth of said trench.

10. The semiconductor integrated circuit device according to Claim 9, further including an implantation region of electrically neutral material.

11. The semiconductor integrated circuit device according to Claim 10, wherein said P-well has diffusion regions within it, and said implantation region of electrically neutral material extends to a depth less than the depth of said diffusion regions.

12. The semiconductor integrated circuit device according to Claim 8, wherein said boron ions have a concentration between approximately 10^{10} atoms/cm^2 and 10^{13} atoms/cm^2.

ABSTRACT

ENHANCED SHALLOW TRENCH ISOLATION (STI) METHOD FOR FABRICATING RADIATION-TOLERANT INTEGRATED CIRCUIT DEVICES

An enhanced shallow trench isolation method for fabricating radiation tolerant integrated circuit devices is disclosed. A layer of pad oxide is first deposited on a semiconductor substrate. A layer of pad nitride is then deposited on the pad oxide layer. A trench is defined within the semiconductor substrate by selectively etching the pad nitride layer, the pad oxide layer, and the semiconductor substrate. Boron ions are then implanted into both the bottom and along the sidewalls of the trench. Subsequently, a trench plug is formed within the trench by depositing an insulating material into the trench and by removing an excess portion of the insulating material. A p-well is implanted to a depth just below the depth of the bottom of the trench. This helps to keep the threshold voltage of the IC device below the trench at a high level, and thereby keep post-radiation leakage low. Then, an electrically neutral species is implanted into the wafer.

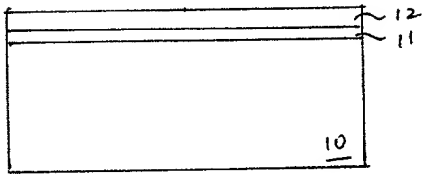

FIGURE 1

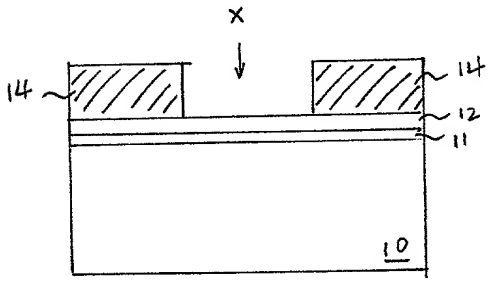

FIGURE 2

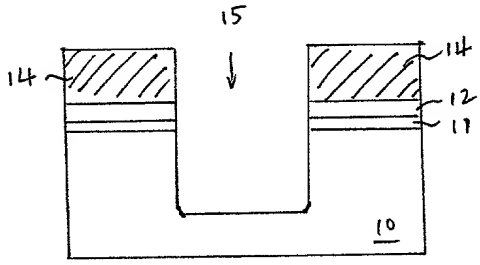

FIGURE 3

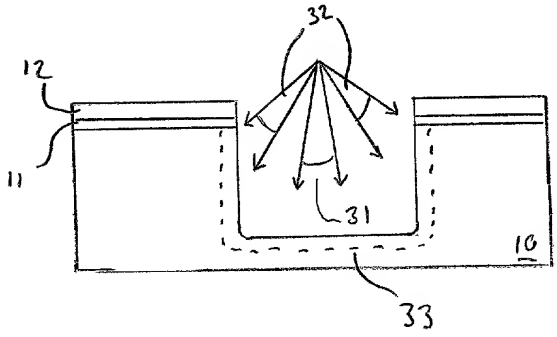

FIGURE 4

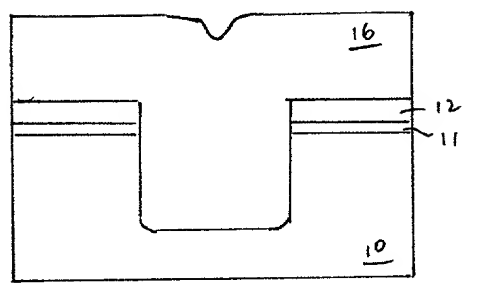

FIGURE 5

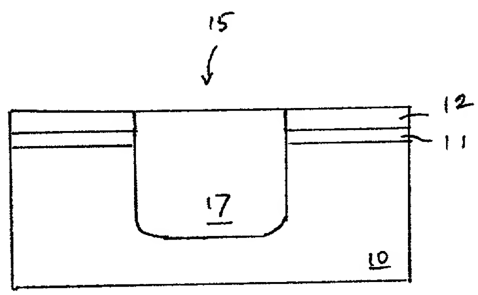

FIGURE 6

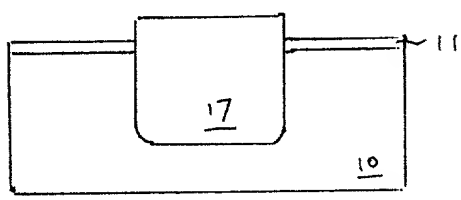

FIGURE 7

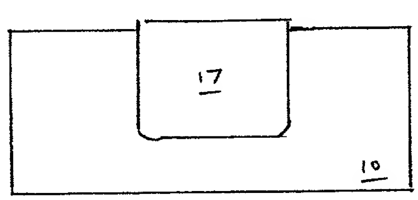

FIGURE 8

CONFIDENTIAL

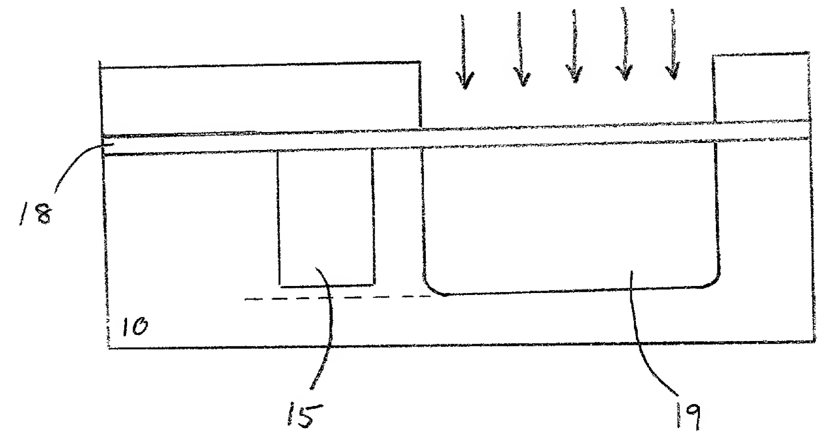

FIGURE 9

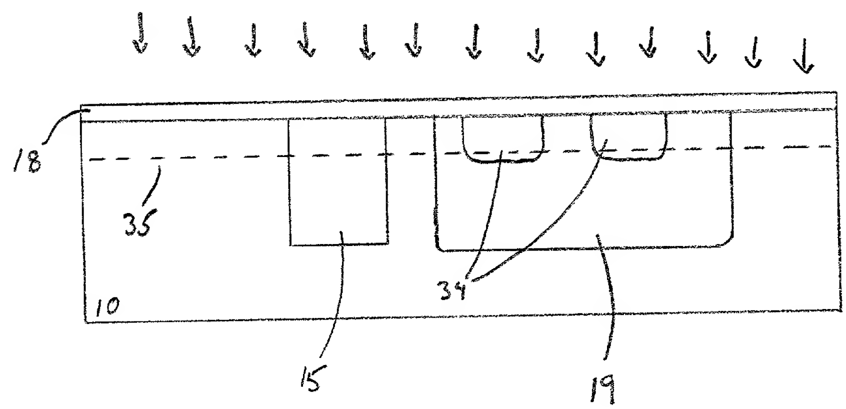

FIGURE 10

COMBINED DECLARATION FOR PATENT APPLICATION AND POWER OF ATTORNEY **(Includes Reference to Provisional and PCT International Applications)**	Attorney's Docket No. 032908-008

As a below named inventor, I hereby declare that:
My residence, post office address and citizenship are as stated below next to my name;
I believe I am the original, first and sole inventor (if only one name is listed below) or an original, first and joint inventor (if plural names are listed below) of the subject matter which is claimed and for which a patent is sought on the invention entitled:

Method to Harden Shallow Trench Isolation Against Total Ionizing Dose Radiation

the specification of which (check only one item below):

☒ is attached hereto.

☐ was filed as United States application
Number _____
on _____
and was amended
on _____ (if applicable).

☐ was filed as PCT international application
Number _____
on _____
and was amended
on _____ (if applicable).

I hereby state that I have reviewed and understand the contents of the above-identified specification, including the claims, as amended by any amendment referred to above.

I acknowledge the duty to disclose to the Office all information known to me to be material to patentability as defined in Title 37, Code of Federal Regulations, §1.56.

I hereby claim foreign priority benefits under Title 35, United States Code, §119 (a)-(e) of any foreign application(s) for patent or inventor's certificate or of any PCT international application(s) designating at least one country other than the United States of America listed below and have also identified below any foreign application(s) for patent or inventor's certificate or any PCT international application(s) designating at least one country other than the United States of America filed by me on the same subject matter having a filing date before that of the application(s) of which priority is claimed:

PRIOR FOREIGN/PCT APPLICATION(S) AND ANY PRIORITY CLAIMS UNDER 35 U.S.C. §119:

COUNTRY (if PCT, indicate "PCT")	APPLICATION NUMBER	DATE OF FILING (day, month, year)	PRIORITY CLAIMED UNDER 35 U.S.C. §119
			_Yes _No
			_Yes _No
			_Yes _No
			_Yes _No
			_Yes _No

I hereby claim the benefit under Title 35, United States Code § 119(e) of any United States provisional application(s) listed below.

60/146,895	2 August 1999
(Application Number)	(Filing Date)
(Application Number)	(Filing Date)

COMBINED DECLARATION FOR PATENT APPLICATION AND POWER OF ATTORNEY (CONT'D) (Includes Reference to Provisional and PCT International Applications)	Attorney's Docket No. 032908-008

I hereby claim the benefit under Title 35, United States Code, §120 of any United States applications(s) or PCT international application(s) designating the United States of America that is/are listed below and, insofar as the subject matter of each of the claims of this application is not disclosed in that/those prior application(s) in the manner provided by the first paragraph of Title 35, United States Code, §112, I acknowledge the duty to disclose to the Office all information known to me to be material to the patentability as defined in Title 37, Code of Federal Regulations §1.56, which became available between the filing date of the prior application(s) and the national or PCT international filing date of this application:

PRIOR U.S. APPLICATIONS OR PCT INTERNATIONAL APPLICATIONS DESIGNATING THE U.S. FOR BENEFIT UNDER 35 U.S.C. §120:

U.S. APPLICATIONS		STATUS *(check one)*		
U.S. APPLICATION NUMBER	U.S. FILING DATE	PATENTED	PENDING	ABANDONED

PCT APPLICATIONS DESIGNATING THE U.S.					
PCT APPLICATION NO.	PCT FILING DATE	U.S. APPLICATION NUMBERS ASSIGNED (if any)			

I hereby appoint the following attorneys and agent(s) to prosecute said application and to transact all business in the Patent and Trademark Office connected therewith and to file, prosecute and to transact all business in connection with international applications directed to said invention:

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I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code and that such willful false statements may jeopardize the validity of the application or any patent issued thereon.

COMBINED DECLARATION FOR PATENT APPLICATION AND POWER OF ATTORNEY (CONT'D) (Includes Reference to Provisional and PCT International Applications)	Attorney's Docket No. 032908-008

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